PATENT ABSTRACTS OF JAPAN

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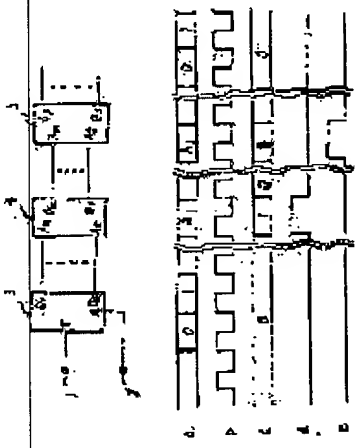
(54) TIMING PULSE GENERATING CIRCUIT

(57)Abstract:
PURPOSE: To decrease the data redundancy by forming two-stage of ROMs as a timing pulse generating circuit in a circuit having a reference clock and a timing pulse and writing only a change point of the timing pulse to the ROMs.
CONSTITUTION: When a pulse is fed to a counter 3 from a reset terminal 2, the count of the counter 3 is zero. When a clock is inputted from a clock input terminal 1, the count of the counter 3 counts up sequentially. A number of a change point of the timing pulse is written in a ROM 4, let the number be 1-q and the other points be '0', then the output of the ROM 4 is as shown in figure c. Data is written so that any of outputs O0-OP of the ROM 5 is '1' with respect to the numbers 1-q in the figure (c), and when the point is '0' in the figure (c), the data is written so that all the outputs O0-OP of the ROM 5 are '0'. Thus, the redundancy of the written data is avoided.



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